each contact comprising a bump having a surface and a plurality of spaced raised portions projecting from the surface [s of the contacts, the raised portions] dimensioned to penetrate into [the] a pad[s] at the force by a penetration depth equal to a height of the raised portions but less than a thickness of the pad[s] while the surface [s of the contacts] limits further penetration into the pad[s], the force selected to be greater than a first force at which the raised portions penetrate the pad[s] but less than a second force at which the [surfaces] bump penetrates the pad. [s, the second force selected to be from two to ten times the first force; and]

[a plurality of conductive traces on the substrate in electrical communication with the contacts and with the external leads.]

93. (four times amended) The apparatus of claim 92 further comprising a plurality of external leads on the plate in electrical communication with the contacts.
[wherein the contacts and the pads are substantially aligned.]

96. (four times amended) The apparatus of claim 92 wherein [each] the raised portions comprise[s a] points.

REMARKS

Rejections Under 35 USC §112

Claims 78-82, 87, 88, 90-93 and 96 have been rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

In response to these rejections, the independent claims have been amended to more clearly relate the location and relationship of the elements. Also, as requested by the

Examiner, a reading of the independent claims on the drawings is as follows.

78. An apparatus **(fixture 11-Figures 1 & 2)** for testing a semiconductor die **(21-Figure 2)** having a plurality of pads **(27-Figures 1-3)** comprising:

a plate **(13-Figures 1 & 2)**;

a substrate **(41-Figures 1 & 2)** on the plate **(13-Figures 1 & 2)** comprising a plurality of contacts **(43-Figures 3 & 4)** configured to electrically contact the pads **(27-Figures 1-3)**;

a clamping mechanism **(89-Figure 8)** attached to the plate **(13-Figure 8)** configured to bias the contacts **(43-Figures 3 & 4)** and the pads **(27-Figures 1-3)** together with a force;

the plate **(13-Figures 1 & 2)**, the substrate **(41-Figure 2)** and the mechanism **(89-Figure 8)** configured such that the die **(21-Figure 2)** can be placed on the substrate **(41-Figure 2)**, the mechanism **(89-Figure 8)** attached to the plate **(13-Figure 8)**, and the die **(21-Figure 2)** retained between the mechanism **(89-Figure 8)** and the substrate **(41-Figure 2)** with the contacts **(43-Figures 3 & 4)** in electrical contact with the pads **(27-Figures 1-3)**; and

each contact **(43-Figures 3 & 4)** comprising a bump **(43 or 61-Figures 4-6)** and a plurality of spaced raised portions **(asperties 69-Figure 4 or raised portions 73-Figure 6)** projecting from the bump **(Figure 4)**, the raised portions **(asperties 69-Figure 4 or raised portions 73-Figure 6)** dimensioned to penetrate into a pad **(27-Figure 4)** at the force to a penetration depth equal to a height of the raised portions **(asperties 69-Figure 4 or raised portions 73-Figure 6)** but less than a thickness of the pad **(27-Figure 4)**, the bump **(43 or 61-Figures 4-6)** dimensioned to limit further penetration of the raised

portions **(asperties 69-Figure 4)** into the pad **(27-Figure 4)** at the force.

87. An apparatus **(fixture 11-Figures 1 & 2)** for testing a semiconductor die **(21-Figure 2)** having a plurality of pads **(27-Figures 1-3)** comprising:

a plate **(13-Figures 1 & 2)** comprising a plurality of external leads **(33-Figures 1 & 2)**;

a substrate **(41-Figures 1 & 2)** on the plate **(13-Figures 1 & 2)** comprising a plurality of contacts **(43-Figures 3 & 4)** configured to electrically contact the pads **(27-Figures 1-3)**;

a clamping mechanism **(89-Figure 8)** attached to the plate **(13-Figure 8)** configured to bias the contacts **(43-Figures 3 & 4)** and the pads **(27-Figures 1-3)** together with a force;

the plate **(13-Figures 1 & 2)**, the substrate **(41-Figure 2)** and the mechanism **(89-Figure 8)** configured such that the die **(21-Figure 2)** can be placed on the substrate **(41-Figure 2)**, the mechanism **(89-Figure 8)** attached to the plate **(13-Figure 8)**, and the die **(21-Figure 2)** retained between the mechanism **(89-Figure 8)** and the substrate **(41-Figure 2)** with the contacts **(43-Figures 3 & 4)** in electrical contact with the pads **(27-Figures 1-3)**; and

each contact **(43-Figures 3 & 4)** comprising a bump **(43 or 61-Figures 4-6)** and a plurality of spaced raised portions **(asperties 69-Figure 4 or raised portions 73-Figure 6)** projecting from the bump **(Figure 4)** with a height, the raised portions **(asperties 69-Figure 4 or raised portions 73-Figure 6)** configured to penetrate into a pad **(27-Figure 4)** with a penetration depth equal to the height but less than a thickness of the pad **(27-Figure 4)** while the bump **(43 or 61-Figures 4-6)** limits further penetration, the force selected to be greater than a first force at which the raised portions **(asperties 69-Figure 4**

or raised portions 73-Figur 6) penetrate the pad **(27-Figure 4)** but less than a second force at which the bump **(43 or 61-Figures 4-6)** penetrate the pad **(27-Figure 4)**, the second force being from two to ten times the first force; and

a plurality of conductive traces **(45-Figures 1 or 4)** on the substrate **(41-Figure 1 or 4)** in electrical communication with the contacts **(43-Figures 3 & 4)** and with the external leads **(33-Figures 1 & 2)**.

92. An apparatus **(fixture 11-Figures 1 & 2)** for testing a semiconductor die **(21-Figure 2)** having a plurality of pads **(27-Figures 1-3)** comprising:

a plate **(13-Figures 1 & 2)** comprising a plurality of external leads **(33-Figures 1 & 2)**;

a substrate **(41-Figures 1 & 2)** on the plate **(13-Figures 1 & 2)** comprising a plurality of contacts **(43-Figures 3 & 4)** configured to electrically contact the pads **(27-Figures 1-3)**;

the plate **(13-Figures 1 & 2)**, the substrate **(41-Figure 2)** and the mechanism **(89-Figure 8)** configured such that the die **(21-Figure 2)** can be placed on the substrate **(41-Figure 2)**, the mechanism **(89-Figure 8)** attached to the plate **(13-Figure 8)**, and the die **(21-Figure 2)** retained between the mechanism **(89-Figure 8)** and the substrate **(41-Figure 2)** with the contacts **(43-Figures 3 & 4)** in electrical contact with the pads **(27-Figures 1-3)**; and

each contact **(43-Figures 3 & 4)** comprising a bump **(61-Figure 6)** having a surface **(Figure 6)** and a plurality of spaced raised portions **(73-Figure 6)** projecting from the surface **(Figure 6)** dimensioned to penetrate into a pad **(27-Figure 6)** at the force by a penetration depth equal to a height of the raised portions **(73-Figure 6)** but less than a thickness of the pad **(27-Figure 6)** while the surface **(Figure 6)** limits further penetration into the pad **(27-**

Figure 6), the force selected to be greater than a first force at which the raised portions **(73-Figure 6)** penetrate the pad **(27-Figure 6)** but less than a second force at which the bump **(61-Figure 6)** penetrates the pad **(27-Figure 6)**.

Antecedent basis for "bump" is provided on page 15, line 24 of the specification.

Antecedent basis for "raised portions" is provided on page 17, line 20 of the specification.

Antecedent basis for "height" is provided on page 15, line 6, of the specification.

Antecedent basis for "force" and "penetration" recitations is provided on page 17, line 25 to page 18-line 15 of the specification.

Rejections Under 35 USC §103

Claims 78-82, 87, 88, 90-93 and 96 have been rejected under 35 USC 103(a) as being unpatentable over Malhi et al (US Patent No. 5,088,190) or Elder et al (US Patent No. 5,123,850) in a first set, in view of Nakano (JP Hei 3-69131) in a second set, and Blonder et al. (US Patent No. 4,937,653) or Bindra et al (US Patent No. 5,137,461) in a third set.

Claims 78-82, 87, 88, 90-93 and 96 have been rejected under 35 USC 103(a) as being unpatentable over Nakano in a first set, in view of Blonder et al. or Bindra et al. in a second set.

The 35 USC §103 rejections are respectfully traversed for the reasons to follow.

Arguments

Malhi et al. '190 and Elder et al. '850 were cited as disclosing test apparatus similar to the present apparatus. However, as recognized by the Examiner, these references do not teach the concept of relating the biasing force produced by a clamping mechanism of the apparatus, to the structure of

contacts on the apparatus, to achieve penetration limitation of pads on the die.

In Elder et al. '850 there is no penetration limitation as contact bumps 24 (Figure 3) are "scrubbed" into the test pads on the die by the compression of the elastomer 25 in the assembled socket (column 4, lines 32-35). In Malhi et al. '190 solder bumps 331, 332, 333, 334 (Figure 3) are designed to mate with pads 301, 302, 303, 305 and make depressions in the pads without penetration (column 6, lines 5-12).

Nakano was cited as teaching a penetration limiting contact. However, Nakano is directed to a method for making a probe card for testing semiconductor dice contained on a wafer (page 2 in Field of Industrial Application). The Nakano probe card replaces a conventional probe card having probe needles (Figures 6 and 7). With a probe card, the biasing force exerted on the probe contacts is controlled by a probe card fixture. Probe cards do not employ clamping mechanisms for generating biasing force, as with the present test apparatus. Accordingly, there is no teaching in Nakano of the concept of relating the biasing force produced by a clamping mechanism, to the geometry of penetrating limiting contacts.

Blonder et al. and Bindra et al. were cited as teaching plural raised portions on a contact structure. However, Blonder et al. is a permanent connection system that requires "bonding of the carrier pads to the chip pads" (col. 2, lines 40-41). Bindra et al. is directed to a separable electrical connection technology that uses interdigitating members 62 adapted to mechanically bond to a solder ball 61 (Figure 20). Neither reference applies a biasing force using a clamping mechanism, and damage to the chip pads during a test procedure is not an issue.

Further, neither the references, nor the prior art, teaches the concept of relating the biasing force produced by a clamping mechanism to the structure of a contact to achieve penetration limitation. Accordingly Applicants would argue

that one skilled in the art at the time of the present invention would have no incentive to combine the references in the manner of the Office Action. As held in ACS Hospital Systems, Inc. v. Montifiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 029, 933 (Fed. Cir. 1984), obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent teaching, suggestion or incentive supporting the combination.

The Examiner states on page 3, last paragraph of the Office Action that:

> "One skilled in the art would realize that the chip and the test probe would have to be held together somehow, as by a clamp mechanism. One skilled in the art would apply a force sufficient to make good contact and not so great as to destroy that being tested. Applicants claimed ranges fall within that category."

Admittedly clamping mechanism are known in the art. However, at the time of the present invention (June 1991) there was no suggestion in the art of the presently claimed clamping mechanism which is configured to operate in combination with a penetration limiting contact structure to provide an improved test apparatus. At the time of the invention it was difficult to make reliable electrical connections without producing at least cosmetic damage to the pads on the die. Thus, while prior art test devices may not have destroyed all the dice being tested, they did not function to make reliable electrical connections with minimal damage to the die as with the present apparatus.

Accordingly, the Examiner is asked to assess the unobviouness of the present invention from the view point of one skilled in the art at the time of the invention. With respect to the cited combination of references, the Examiner is asked to review the teachings of the references and the prior art, without the benefit of the present disclosure, for motivation for the cited combination. The Applicants would

submit that neither the references, nor the prior art, provides such a motivation.

In view of the amendments and arguments, it is submitted that amended claims 78-82, 87, 88, 90-93 and 96 are now in a condition for allowance. Should any other issues remain, it is requested that the Examiner contact the undersigned attorney.

DATED this 16th day of May, 2000.

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May 16, 2000
Date of Signature

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